UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/632,195 | 07/31/2003 | Chun-Hung Lin | JCLA7907-CA | 9823 |

23900 7590 05/31/2005

J C PATENTS, INC.
4 VENTURE, SUITE 250
IRVINE, CA 92618

| EXAMINER | |
|---|---|
| PEUGH, BRIAN R | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2187 | |

DATE MAILED: 05/31/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/632,195 | LIN ET AL. | |
| | Examiner | Art Unit | |
| | Brian R. Peugh | 2187 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *16 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,4,6 and 9-15* is/are rejected.

7)☒ Claim(s) *2,5,7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/28/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Information Disclosure Statement*

The information disclosure statement (IDS) submitted on October 28, 2004 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

### *Response to Amendment*

This Office Action is in response to applicant's communication filed March 16, 2005, in response to PTO Office Action dated March 3, 2005. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-15 have been presented for examination in this application. In response to the last Office Action, claims 16-22 have been cancelled.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3, 4, and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang et al. (US# 5,901,086).

Regarding claim 1, Wang et al. teaches **a read method to a flash memory** (10) **from a data-access requesting component** [instruction sequences sent to memory inherently requires sender; col. 3, lines 29-31], **wherein the flash memory includes a plurality of storage sectors** [memory cells; col. 2, lines 52-62], **and a read operation to one sector of the storage sectors needs a plurality of stages handled by an access controller** [col. 2, lines 29-34], **the reading method comprising: Performing a read operation to read a current sector of the storage sectors** [Fig. 2; col. 3, lines 51-56]; **and starting to perform a second read operation to a next sector of thee storage sectors when the first read operation is not completed yet** [col. 3, lines 57-60; col. 4, lines 7-11]; **wherein the second read operation starts before the first read operation ends thereby decreasing the time required to perform read operations and increasing overall system performance** [col. 4, lines 7-11 & 38-41].

Regarding claim 3, Wang et al. teaches **wherein the stages includes a first stage for finding a sector of the storage sectors to be read** [stage 1 corresponds to col. 3, lines 51-56; Fig. 2, ADD of time T2], **a second stage for transmitting an information to be read from the flash memory into the access controller** [stage 2 corresponds to col. 3, lines 57-60; Fig. 2, time T3]; **and a third stage for transmitting an information to be read in the access controller into the data-access requesting**

**component** [stage 3 corresponds to col. 3, line 66 – col. 4, line 2; Fig. 2, DATA OUTPUT of T2,T3,T0].

Regarding claim 4, Wang et al. teaches **recurrently performing the foregoing steps if another sector is still to be read** [Fig. 2; col. 4, lines 7-11 & 36-41].

Regarding claim 6, Wang et al. teaches **wherein the third stage for the first read operation is overlapping with the second stage for the second read operation** [Fig. 2; 3rd stage of read op. 1 (T2,T3,T0) overlaps 2nd stage of read op. 2 (T3)].

Claims 9-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Fandrich et al. (US# 5,519,847).

Regarding claim 9, Fandrich et al. teaches **a writing method to a flash memory** [Fig. 2, (20)] **from a data-access requesting component, wherein the flash memory includes a plurality of storage sectors** [memory cells; col. 2, lines 63-64], **and a writing operation to one sector of the storage sectors needs a plurality of stages handled by an access controller, the writing method comprising** [col. 1, lines 56-59]: **performing a first writing operation to write a current sector of the storage sectors** [col. 6, lines 19-26; Fig. 6, (404); Fig. 8, T1-T2 sequence]; **and starting to perform a second writing operation to a next sector of the storage sectors when the first writing operation is not completed yet** [col. 6, lines 57-61; Fig. 6, (406); Fig. 8, T2-T3 sequences, upper sequence for 2nd writing op., lower sequence for 1st writing op.] ; **wherein the second writing operation starts before the first writing operation**

**ends thereby decreasing the time required to perform writing operations and increasing the overall system performance** [col. 1, lines 49-67; start of 2nd op. (upper T2-T3 sequence) occurs during writing of 1st op. (450), lower T2-T3 sequence].

Regarding claim 10, Fandrich et al. teaches **starting to perform a third writing operation** [Fig. 8, T3-T4 upper sequence] **to write a further next sector of the storage sectors when the second writing operation is not completed yet** [Fig. 8, T3-T4 lower sequence].

Regarding claim 11, Fandrich et al. teaches **wherein the stages includes a first stage for transmitting an information to be written into the access controller** [col. 6, lines 19-26], **a second stage for finding a sector of the storage sectors in the flash memory to be written** [col. 6, lines 57-61] **and a third stage for transmitting an information in the access controller into the flash memory** [col. 6, lines 62-66] [In Fig. 8, upper sequence 'Load Plane (A or B) & Give Program Command' corresponds to stages 1 & 2; lower sequence 'Program from Plane (A or B)' corresponds to stage 3].

Regarding claim 12, Fandrich et al. teaches **recurrently performing the foregoing steps if another sector is sill to be written** [Fig. 6, step (410); col. 7, lines 35-40].

Regarding claim 13, Fandrich et al. teaches **wherein the third stage for the first writing operation is overlapping with the first stage of the second writing operation** [In Fig. 8, upper sequence 'Load Plane (A or B) & Give Program Command'

corresponds to stages 1 & 2; lower sequence 'Program from Plane (A or B)' corresponds to stage 3].

Regarding claim 14, Fandrich et al. teaches **wherein the first stage and the second stage for the same writing operation are overlapping** [In Fig. 8, upper sequence 'Load Plane (A or B) & Give Program Command' corresponds to stages 1 & 2].

Regarding claim 15, Fandrich et al. teaches **wherein the third stage of the first writing operation, the first stage for the second writing operation, and the second stage for the second writing operation are overlapping** [In Fig. 8, upper sequence 'Load Plane (A or B) & Give Program Command' corresponds to stages 1 & 2; lower sequence 'Program from Plane (A or B)' corresponds to stage 3].

### *Allowable Subject Matter*

Claims 2, 5, 7, and 8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

### *Conclusion*

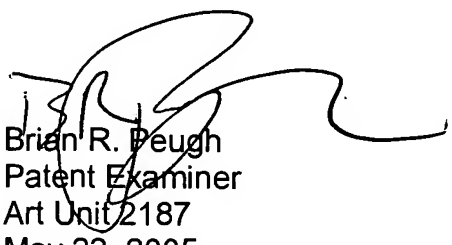
The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The prior art corresponds to related pipelining systems.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is (571) 272-4199. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks, can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Brian R. Peugh
Patent Examiner
Art Unit 2187
May 22, 2005